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# APPLICATION FOR LETTERS PATENT

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# Methods Of Treating Regions Of Substantially Upright Silicon-comprising Structures, Methods Of Treating Silicon-comprising Emitter Structures, Methods Of Forming Field Emission Display Devices, And Cathode Assemblies

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INVENTOR

Ammar Derraa

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# Methods Of Treating Regions Of Substantially Upright Silicon-comprising Structures, Methods Of Treating Silicon-comprising Emitter Structures, Methods Of Forming Field Emission Display Devices, And Cathode Assemblies

## PATENT RIGHTS STATEMENT

This invention was made with Government support under Contract No. DABT63-97-C-0001 awarded by Advanced Research Projects Agency (ARPA). The Government has certain rights in this invention.

## TECHNICAL FIELD

The invention pertains to methods of treating substantially upright silicon-comprising structures, such as, for example, methods of treating silicon-comprising emitter structures. In particular aspects, the invention pertains to methods of forming field emission display devices. In other particular aspects, the invention pertains to cathode assemblies.

## BACKGROUND OF THE INVENTION

Silicon-comprising field emitters are currently being designed and incorporated into field emission display devices, and show promise as candidates for electron sources in vacuum microelectronic devices. It is generally desirable to fabricate the emitters to have tips that are as sharp as possible, as such can improve control of electron emission from the tips. For instance, clarity, or resolution, of a field emission display is a function of, among other things, emitter tip sharpness. As sharper

emitter tips can produce higher resolution displays than less sharp emitter tips, numerous methods have been proposed for fabrication of very sharp emitter tips (i.e., emitter tips having tip radii of 100 nanometers or less).

Fabrication of very sharp tips has, however, proved difficult. Accordingly, other methods, besides simply sharpening emitter tips, have been proposed for improving electron emission from emitters. Among such other methods are procedures for treating silicon-comprising emitters to convert the silicon to porous silicon, and procedures for treating silicon-comprising field emitters to coat the emitters with materials having lower work function properties than silicon. Such materials include, for example, diamond, cesium (such as, for example, cesiated carbon) and boronitride (the boronitride can be undoped, or doped with, for example, sulfur).

The above-discussed procedures of treating silicon-comprising emitters show promise for improving emission from individual emitters, as well as for improving uniformity of emission across arrays of emitters. Accordingly, it would be desirable to develop methods of fabricating emitters wherein emitter treatments are incorporated into the emitter fabrication processes.

## SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of treating the end portions of an array of substantially upright silicon-comprising structures. A substrate having a plurality of substantially upright silicon-comprising structures extending thereover is provided. The substantially upright silicon-comprising structures have base portions, and have end portions above the base portions. A masking layer is formed over the substrate to cover the base portions of the substantially upright silicon-comprising structures while leaving the end portions exposed. While the masking layer covers the base portions, the end portions are exposed to conditions which alter the end portions relative to the base portions.

In another aspect, the invention encompasses a method of treating the ends of an array of silicon-comprising emitter structures. A substrate having a plurality of silicon-comprising emitter structures thereover is provided. The emitter structures have base portions and ends above the base portions. A layer of spin-on-glass is formed over the substrate. The layer of spin-on-glass covers the base portions of the emitter structures and leaves the ends exposed. While the layer of spin-on-glass covers the base portions, the ends are exposed to conditions which alter the ends relative to the base portions.

In yet another aspect, the invention encompasses a cathode assembly which includes a plurality of silicon-comprising emitter structures projecting over a substrate. The emitter structures have base portions

and ends above the base portions, and the ends comprise a different material than the base portions.

## BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic, cross-sectional, fragmentary view of a portion of an emitter array assembly illustrated at a preliminary step of a method of the present invention.

Fig. 2 is a view of the Fig. 1 assembly shown at a processing step subsequent to that of Fig. 1.

Fig. 3 is a view of the Fig. 1 assembly shown at a processing step subsequent to that of Fig. 2.

Fig. 4 is a view of the Fig. 1 assembly shown at a processing step subsequent to that of Fig. 1 in accordance with a second embodiment method of the present invention.

Fig. 5 is a view of the Fig. 4 assembly shown after a first embodiment treatment process.

Fig. 6 is a view of the Fig. 4 assembly shown after a second embodiment treatment process.

Fig. 7 is a fragmentary, diagrammatic, cross-sectional view of a field emission display incorporating the treated emitters of Fig. 6.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

In one aspect, the invention encompasses methods of treating portions of substantially upright silicon-comprising structures (such as, for example, silicon-comprising emitter structures), while leaving other portions untreated. In particular embodiments, the methodology can be utilized for treating tip regions (i.e., apexes) of silicon-comprising emitter structures, while leaving base regions untreated. Such can advantageously enable modification of electron emitting portions of emitter structures, while not altering physical properties of underlying portions of the emitter structures. Specific embodiments are described with reference to Figs. 1-6.

Referring to Fig. 1, a fragment 10 of a semiconductive material construction is illustrated at a preliminary step of a method of the present invention. Fragment 10 comprises a glass plate 12, a first semiconductive material layer 14 overlying glass plate 12, and emitter structures 20 overlying first semiconductive material layer 14. Emitter structures 20 comprise a second semiconductive material 16. Semiconductive material 14 can comprise either p-type doped or n-type doped semiconductive material, (such as, for example, monocrystalline silicon), and semiconductive material 16 can comprise doped

polycrystalline silicon (polysilicon) material, or, in specific embodiments, consist essentially of conductively doped polysilicon. Materials 12, 14 and 16 together comprise a conventional emitter tip array construction, and can be formed by conventional methods.

To aid in interpretation of this disclosure and the claims that follow, it is noted that layer 14 can be referred to as a "semiconductive substrate". More specifically, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Emitter structures 20 represent a portion of an array of emitter structures. Such array can be referred to as a "cathode array," as the emitters can be incorporated as cathodes in electron emission devices. Each of emitter structures 20 is a substantially upright silicon-comprising structure comprising a base portion 22 and an end portion 24 above the base portion (end portion 24 can also be referred to as an apex, or tip).

A next aspect of the shown exemplary embodiment comprises forming a masking layer over base portions 22 to protect base portions 22 from subsequent conditions. Exemplary methods for forming the masking layer are described with reference to Figs. 2-4, with Figs. 2

and 3 illustrating a first embodiment method, and Fig. 4 illustrating a second embodiment method.

Referring to Fig. 2, a masking layer 30 is provided over semiconductive material 14 and over emitter structures 20. Masking material 30 is preferably provided to be thinner over apexes 24 than over base regions 22. Such can be accomplished, for example, by applying material 30 as a liquid. Exemplary processes include applying material 30 through spin-on-glass methodologies, or through so-called "Flowfill™" methodologies. In Flowfill™ methodologies, material 30 is initially provided as silanol (or an organic derivative of silanol). The silanol can be subsequently converted to silicon dioxide through conventional treatment methodologies.

Referring to Fig. 3, material of layer 30 is removed from over apexes 24, but left over base regions 22. In embodiments in which layer 30 comprises either spin-on-glass or silicon dioxide, such can be accomplished by dipping apexes 24 in a hydrofluoric acid-comprising material. For instance, if material 30 comprises spin-on-glass having a thickness of less than 50 Å over apexes 24, the selective removal of material 30 from over apexes 24 can comprise a dip in a hydrofluoric acid solution for about five seconds.

Referring to Fig. 4, another method of applying material 30 over emitters 20 is to utilize conditions which form material of layer 30 only over base regions 22, and not over apexes 24. Such conditions can

include applying material of layer 30 as a liquid, and adjusting the viscosity of such liquid to effectively have the material run off the steep surfaces of apexes 24. The liquid material of layer 30 then collects over layer 14 to a level which covers base regions 22.

Regardless of whether the embodiment of Figs. 2 and 3 is utilized, or the embodiment of Fig. 4 is utilized, the result is a construction having base regions 22 of emitters 20 protected by a masking layer 30, while apexes 24 are exposed through the masking layer 30.

Figs. 5 and 6 illustrate methods of treating apexes 24 with conditions which alter apex regions 24 relative to base regions 22. Fig. 5 illustrates first embodiment processing conditions, and Fig. 6 illustrates second embodiment processing conditions.

Referring to Fig. 5, a low work function material 40 is provided over apex regions 24 and over masking layer 30. The term "low work function" is used herein to refer to materials having lower work functions than material 16. As discussed above, in particular applications material 16 comprises silicon. In such particular applications "low work function" can refer to materials having lower work functions than silicon. In applications in which material 16 comprises silicon, low work function material 40 can comprise, for example, diamond, cesium (such as, for example, cesiated carbon) or boronitride (such as, for example, sulfur doped boronitride). The provision of low work function material 40 over and against apexes 24 can alter electron emission properties of

emitters 20. Specifically, low work function material 40 can increase electron emission across the array of emitters 20. By selectively forming low work function material 40 only against apexes 24, and not against base regions 22, the methodology of the present invention can avoid adversely affecting physical properties of base region 22 with the low work function material of layer 40. Potential adverse effects that could occur if low work function material 40 were provided against base region 22 include spurious electron emission from the base regions of emitters 20. Accordingly, the selective provision of low work function material 40 over only apexes 24 of emitters 20 can form improved emitter devices relative to devices having low work function material provided over an entire surface (i.e., both a base region and an apex region) of an emitter structure.

After formation of low work function material 40 over apexes 24, the construction 10 can be incorporated into, for example, a field emission display device. Masking material 30 and low work function material 40 can be removed from between emitters 20 prior to incorporation in the device. Such removal can be accomplished by, for example, photolithographic processing wherein a photoresist mask is utilized to protect apexes 24 while materials of layers 30 and 40 are etched from between the apexes. Suitable etching conditions can include, for example, HF based solutions or other etchants depending on the low work function material.

Referring to Fig. 6, an alternative method of treating apex regions 24 is illustrated. Specifically, apex regions 24 have been subjected to processing which forms porous silicon (represented by stippling in Fig. 6) within the apex regions. Such formation of porous silicon can increase electron emission and improve uniformity across an array of emitters 20, and can also improve a quality of electron emission from individual emitters 20 of the array. The formation of porous silicon at tip regions 24 can be accomplished by exposing fragment 10 to electrochemical etching in the presence of hydrofluoric acid. During such exposure, layer 30 protects base portions 22 so that apex regions 24 are rendered more porous than base portions 22 by the electrochemical etching. The electrochemical etching procedure can vary depending on whether silicon-comprising material 16 of emitter structures 20 is doped with an n-type material or a p-type material. Specifically, if silicon-comprising material 16 is doped with an n-type material, tip regions 24 are preferably exposed to light during the electrochemical etching. The light can be generated by, for example, a tungsten lamp. If, on the other hand, silicon-comprising material 16 is doped with a p-type material, the electrochemical etching preferably occurs in the dark.

After tip regions 24 have been rendered porous, masking layer 30 can be removed. Methods for removing masking layer 30 can include, for example, photolithographic processing wherein photoresist blocks are formed to protect apex regions 24. Subsequently, the material of

layer 30 that is between apex regions 24 is exposed to etching conditions which remove such material from over silicon-comprising layer 14. The etching conditions can include, for example, HF based solutions or other etchants depending on the masking material.

Fig. 7 illustrates the porous tipped emitter devices 20 of Fig. 6 incorporated into a field emission display device 70. Field emission display device 70 includes dielectric regions 72, spacers 73, an extractor 74, and a luminescent screen 76. Screen 76 is associated with a face plate 80, and emitters 20 are part of a base plate structure 82. Device 70 is constructed with face plate 80 spaced from base plate 82. Techniques for forming field emission displays are described in U.S. Pat. Nos. 5,151,061; 5,186,670 and 5,210,472; hereby expressly incorporated by reference herein.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.